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PLATING METHOD AND PLATING APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention:

[0001] The present invention relates to a plating method and a plating apparatus, and more particularly to a plating method and a plating apparatus for filling a metal such as copper (Cu) or the like into fine interconnection patterns (trenches) on a semiconductor substrate.

Description of the Related Art:

[0002] Aluminum or an aluminum alloy has generally been used as a material for forming interconnect circuits on semiconductor substrates. As integrated density has increased in recent years, there is a demand for usage of a material having a higher conductivity as an interconnect material. It has been proposed to plate a substrate having interconnect pattern trenches thereon to fill the trenches with copper or its alloy.

15 [0003] There are known various processes including CVD (chemical vapor deposition), sputtering, and the like to fill interconnect pattern trenches with copper or its alloy. However, the CVD process is costly for forming copper interconnections, and the sputtering process fails to embed copper or its alloy in interconnect pattern trenches when the interconnect pattern trenches have a high aspect ratio, i.e., a high ratio of depth to width.

20 A plating process is most effective to deposit a metal layer of copper or its alloy on a substrate to form copper interconnections thereon.

[0004] Various processes are available for plating semiconductor substrates with copper. These include a process of immersing a substrate in a plating liquid held at all times in a plating tank, referred to as a cup-type or dipping-type process; a process of holding a plating liquid in a plating tank only when a substrate, to be plated, is supplied to the plating tank; an electric plating process for plating a substrate with a potential difference; and an electroless plating process for plating a substrate with no potential difference.

[0005] In carrying out filling of fine interconnect patterns with copper by electric

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